Docket No.: BUR920010098

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Devins et al,) Examiner: ALHIJA, SAIF A.
)
Serial No.: 09/683,677) Art Unit: 2128
)
Filing Date: 02/01/2002)
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Title: METHOD OF SWITCHING EXTERNAL MODELS IN AN AUTOMATED SYSTEM-ON-CHIP INTEGRATED CIRCUIT DESIGN VERIFICATION SYSTEM

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 C.F.R. '1.132

Sir:

I, Robert J. Devins, hereby declare as follows:

1. I received a B.S. degree in computer science from the State University of New York in 1979.

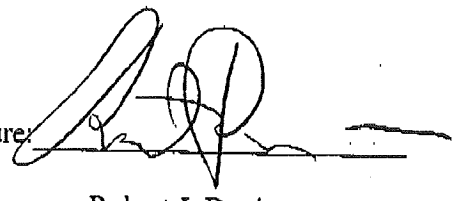
2. I am an inventor in the above-indicated application for a patent. As an inventor, I am thoroughly familiar with the subject matter "Method of Switching External Models in an Automated System-on-Chip Integrated Circuit Design Verification System" which is described and claimed in the present invention.

3. I am an author the paper "An embedded PowerPC SOC for Test and Measurement Applications", IEEE, 2000 cited by the Examiner in an Office Communication mailed on 08/13/2007.

4. I have practiced design verification for International Business Machines Corporation, the assignee in the above-indicated application for a patent, since 1981. The Invention includes first models connected between the simulated system-on-chip (SOC) and a simulated external memory mapped test device (EMMTD) having a simulated switch. The switch selectively connects second models between the EMMTD and the SOC. I declare that the referenced IEEE paper "An embedded PowerPC SOC for Test and Measurement Applications" does not teach nor was intended to teach an EMMTD having a simulated switch. The simulated external memory mapped test device of the referenced IEEE paper does not contain any means for selecting models to connect between the EMMTD and the SOC.

5. I hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date 9/26/07

Signature: 

Robert J. Devins